CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a plurality of multiplexers to select one of a positive transmitter pin and a negative transmitter pin; and

a first comparator to compare a voltage of the selected pin with a first reference voltage to determine whether leakage exists at the selected pin.

2. The semiconductor device of claim 1, further comprising core logic circuitry to receive an output of the first comparator.

3. The semiconductor device of claim 1, further comprising:

a first plurality of termination resistors coupled to the positive transmitter pin; and

a second plurality of termination resistors coupled to the negative transmitter pin such that each of the first and second pluralities of termination resistors are tested with the first reference voltage and the first comparator.

4. The semiconductor device of claim 1, further comprising a positive receiver pin and a negative receiver pin coupled to the positive and negative transmitter pins, respectively, to provide an analog loop back path.

5. The semiconductor device of claim 4, further comprising:

a second plurality of switches operable to select one of the positive and negative receiver pins to be charged up; and

a second comparator coupled to the receiver to compare the charged up receiver pin with a second reference voltage to determine whether leakage exists at the charged up receiver pin.

6. The semiconductor device of claim 5, wherein the second plurality of switches are operable to select the second reference voltage from the plurality of voltage supplies.

7. A semiconductor device comprising:

a plurality of switches operable to select one of a positive receiver pin and a negative receiver pin to be charged up; and

a comparator coupled to the receiver to compare the charged up receiver pin with a reference voltage to determine whether leakage exists at the charged up receiver pin.

8. The semiconductor device of claim 7, wherein the plurality of switches are operable to select the reference voltage from a plurality of voltage supplies.

9. A method to test an input/output of a semiconductor device, the method comprising:

selecting a positive transmitter pin or a negative transmitter pin; and

comparing a voltage at the selected transmitter pin with a first reference voltage using a first comparator in the semiconductor device to determine whether leakage exists at the selected transmitter pin.

10. The method of claim 9, further comprising selecting the first reference voltage out of a plurality of voltage supplies.

11. The method of claim 10, further comprising:

selecting one or more of a plurality of termination resistors; and

testing the selected termination resistors with the first reference voltage and the first comparator.

12. The method of claim 9, further comprising:

coupling a positive receiver pin and a negative receiver pin in the semiconductor device to the positive and negative transmitter pins, respectively, to provide an analog loop back path within the semiconductor device; and

sending a test pattern from the positive and negative transmitter pins to the positive and negative receiver pins.

13. The method of claim 12, further comprising:

charging up one of the positive and negative receiver pins; and

comparing a voltage of the charged up receiver pin with a second reference voltage using a second comparator within the semiconductor device to determine whether there is leakage at the charged up receiver pin.

14. The method of claim 13, further comprising selecting the second reference voltage from the plurality of voltage supplies.

15. A method to test a transmitter and a receiver of a semiconductor device, the method comprising:

coupling a plurality of switches to a transmitter termination resistor, a receiver termination resistor, and a transmitter current driver;

closing one or more of the plurality of switches to select a different effective capacitance between the transmitter and the receiver during testing.

16. The method of claim 15, wherein closing the one or more of the plurality of switches allows an external capacitor to provide part of an effective capacitance during testing.

17. The method of claim 15, wherein closing the one or more of the plurality of switches allows a plurality of trace lines having a parasitic capacitance to provide part of an effective capacitance during testing.

18. A computer system comprising:

a plurality of dynamic random access memory devices (DRAM); and

a chipset coupled to the plurality of DRAMs, the chipset including a semiconductor device that comprises

a plurality of multiplexers to select one of a positive transmitter pin and a negative transmitter pin; and

a first comparator to compare a voltage of the selected pin with a first reference voltage to determine whether leakage exists at the selected pin.

19. The computer system of claim 18, wherein the semiconductor device further comprises:

a first plurality of termination resistors coupled to the positive transmitter pin; and

a second plurality of termination resistors coupled to the negative transmitter pin such that each of the first and second pluralities of termination resistors can be tested using the first reference voltage and the first comparator.

20. The computer system of claim 18, wherein the semiconductor device further comprises a positive receiver pin and a negative receiver pin coupled to the positive and negative transmitter pins, respectively, to provide an analog loop back path.

21. The computer system of claim 20, wherein the semiconductor device further comprises:

a second plurality of switches operable to select the positive receiver pin or the negative receiver pins to be charged up; and

a second comparator coupled to the receiver to compare the charged up receiver pin with a second reference voltage to determine whether leakage exists at the charged up receiver pin.

22. The computer system of claim 18, wherein the semiconductor device is a memory controller.

23. The computer system of claim 18, wherein the semiconductor device is an input/output controller.

24. The computer system of claim 18, further comprising a processor coupled to the chipset.